MOTOROLA
Semiconductor Products Inc.

AN-845
Application Note

NEW POWER BIPOLARS COMPARE FAVORABLY WITH FETs FOR SWITCHING EFFICIENCY

INTRODUCTION

Power MOSFETs are recognized as being extremely fast switching devices, but are they more efficient than bipolars in all or many high voltage switching applications? The answer is — it depends. Efficiency is a measure of dissipation, which, in switchmode circuits, consists primarily of switching losses, both turn-off and turn-on, and saturation losses. Since switching losses are a function of the switching frequency and saturation losses are relatively constant, there reaches a point in the frequency spectrum where one loss predominates over the other. Thus, in low frequency applications, devices with low saturation or ON voltage would show lower losses as measured by the device case temperature and at high frequencies, the fast switchers would run cooler.

TEMPERATURE TESTING

The foregoing has been illustrated by temperature testing three different high voltage switching transistors — the 2N6545 which was one of the first transistors characterized for switchmode applications; the MJ16004, a state-of-the-art switchmode transistor designed for higher frequency operation; and the Power MOSFET MTM5N40. All these devices are of similar die size, voltage and current ratings (Table 1) and were tested with nearly identical loads.

Since the input drive for both turn-on and turn-off can be chosen to optimize the switching speed, the drives selected were those generally shown on the data sheet; i.e., forced gains of 5 and 7 respectively for the 2N6545 and the MJ16004 and off-bias voltages of -5.0 V and -2.0 V; gate drive of greater than 10 V for the MTM5N40.

Resistive loads were chosen for the temperature rise versus frequency test since the load current could be maintained at a constant 2.5 A (R_L = 20 Ω, 50 W, V_{CC} = V_{DD} = 50 V) as the frequency was varied. Recognizing that the "real world" load is usually inductive and that inductive turn-off switching losses are greater than turn-on due to the rectangular load line, a single frequency (75 kHz) inductive test was also run. Due to the different ON voltages and turn-off times for the bipolars and MOSFET, the load inductances had to be slightly different to achieve the same peak collector (drain) currents for a normalized test. For the 75 kHz test, the peak ramp current of about 3.0 A peak was achieved with inductances of 32 μH and 27 μH respectively when V_{CC} and V_{DD} were +16 V.

TABLE 1. Specifications of DUTs

	SMI 2N6545	SMIII MJ16004	TMOS MTM5N40
Die Size (Area)	160×160 mil (25600 mil^2)	157×157 mil (24649 mil^2)	126×182 mil (22932 mil^2)
I_C, I_D	8.0 A	5.0 A	5.0 A
V_{CEO}, V_{DDS}	400 V	450 V	400 V
$V_{CE(sat)max}$, $V_{DS(sat)max}$	1.5 V @ 5.0 A	2.5 V @ 3.0 A	4.5 V @ 3.0 A, $r_{DS(on)}$ max = 1.5 Ω
$V_{CE(sat)typ}$, $V_{DS(sat)typ}$	0.3 V	0.3 V	3.3 V @ 1.1 Ω
$h_{FE(min)}$, $g_{fs(min)}$	7.0 @ 5.0 A	7.0 @ 5.0 A	2.0 mhos @ 2.5 A

Published with permission of Power Conversion International

The temperature rise test fixture (Figure 1) consists of a clocked, three-phase counter sequentially driving the three respective switching circuits; thus, each Device Under Test (D.U.T.) is driven at a 33% duty cycle. However, at high frequencies (low on times), DUTs with greater storage times will effectively be powered for longer duty cycles and therefore have greater saturation losses contributing to the device temperature rise. As an example, at 150 kHz (period of 6.7 μs) the 33% dc drive on-time of about 2.2 μs would result in about 48% power on-time with only 1.0 μs of storage time.

The clocks for this system, one for the resistive load case and the other for the inductive load, consist of two CMOS gate configured RC astable multivibrators. Switchable timing capacitors set the frequencies for the resistive load at 5, 25, 75 and 150 kHz respectively; the inductive load clock is set at a fixed frequency of 75 kHz. The outputs of these MV's clock the MC14022 Octal Counter Divider connected as a three-phase ring counter whose respective emitter follower, positive-going outputs control the three virtually identical drivers.

Forward base current for the bipolars is set by turning on the NPN transistors Q2 and Q7 and the following PNP transistors Q3 and Q8. To minimize storage time, Q3 and Q8 are fashioned as constant current generators, supplying the base currents to the 2N6545 ($\beta_F = 5$, $I_{B1} \cong 600$ mA) and MJ16004 ($\beta_F = 7$, $I_{B1} \cong 430$ mA) for the inductive load current of 3.0 A peak. Forward gate voltage for the power MOSFET is generated by turning on PNP transistor Q13 (Baker clamped to minimize t_s) and thereby applying nearly the full 15 V rail voltage to the gate. The 15 Ω current limiting resistor provides the low source impedance for quickly charging (and thus switching) the MOSFET input capacitance C_{iss}.

Reverse bias voltage $V_{BE(off)}$ or $V_{GS(off)}$), for rapidly turning off the DUTs, are derived by differentiating the input pulse with the resistor-capacitor networks in the base circuits of Q4, Q9 and Q14. The resulting negative going pulses, which are coincident with the trailing edge of the input pulse, then turns on the following respective PNP transistors Q4, Q8 and Q13 for about 3.0 μs. These transistors then turn on NPN transistors Q5, Q10 and Q15 whose emitters are referenced to a

FIGURE 1 — TEMPERATURE RISE FIXTURE SMI, SMIII, TMOS

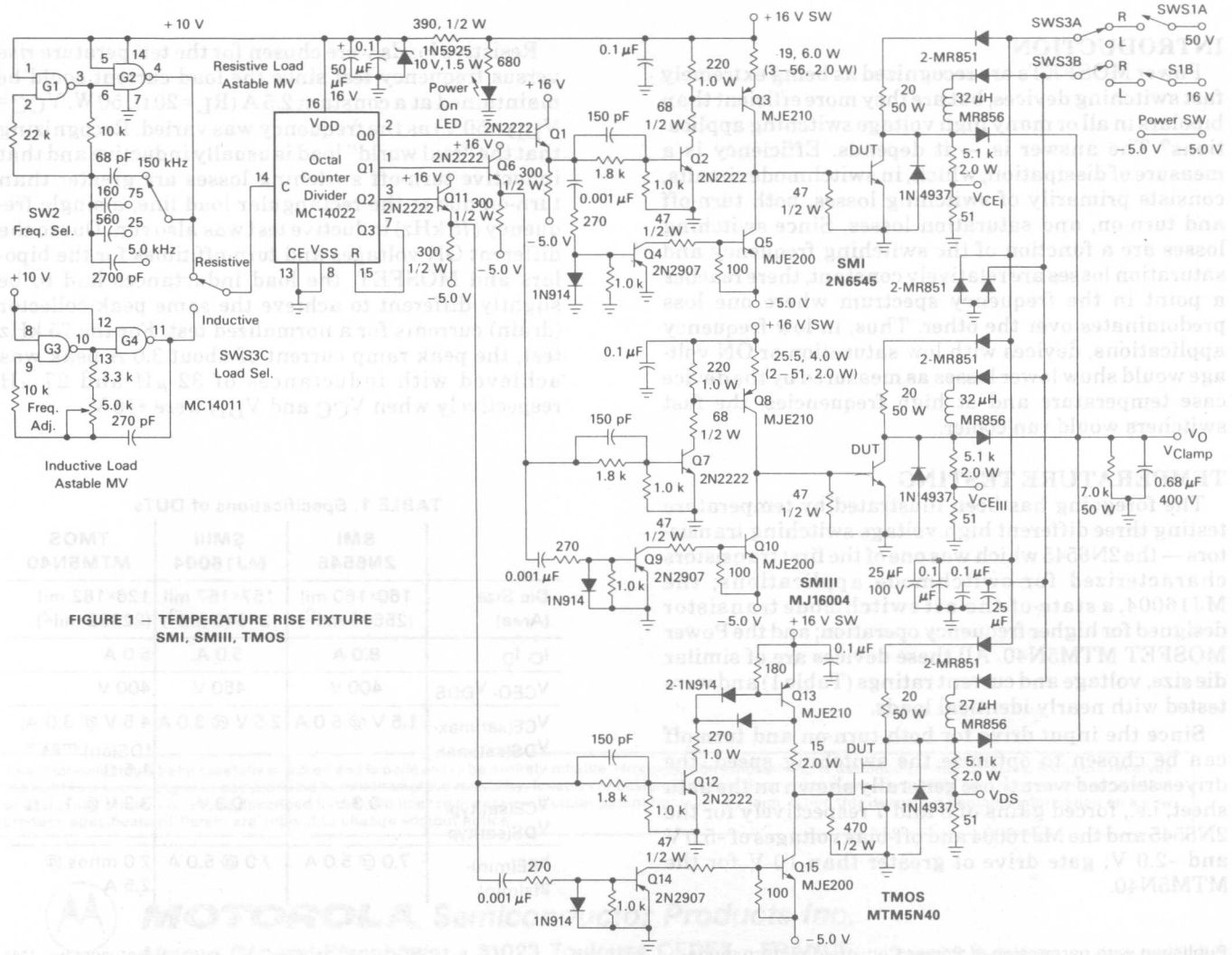


FIGURE 1 — TEMPERATURE RISE FIXTURE SMI, SMIII, TMOS

negative power supply; thus, the reverse bias voltages and resulting reverse bias currents (I_{B2} for bipolars) are applied to the DUT for the 3.0 μs immediately following the turn-on pulse. This reverse bias voltage can then be varied to determine its effect on switching speeds, power dissipation and case temperature rise. For the following described temperature tests, the bias voltages were set for -2.0 V and -5.0 V respectively, the presumed optimum values that are listed in the respective data sheets.

The resistive loads, being somewhat inductive wirewound resistors, have turn-on switching current rise times limited by the L/R time constant (Figure 2) and thus independent of input drive. However, the turn-off voltage and current switching times are affected by off-bias (Figure 3); thus at optimum bias voltage, the switching losses and therefore case temperature can be minimized. This is quite evident in the curves of Figure 4 showing temperature rise versus frequency at two off-bias voltages. All three devices showed slightly lower case temperatures (1 to 3°C) when the optimum off-bias was used at the higher frequencies where switching losses predominate.

The Power MOSFET also runs cooler at higher off-bias voltage. This is due to the charged input capacitance C_{iss} being discharged more quickly when clamped to a greater negative voltage; thus the turn-off switching speeds are improved.

As expected at low frequencies, where On losses predominate, both the 2N6545 (Switchmode I-SMI) and the MJ16004 (SMIII) have temperature rises proportional to $V_{CE(sat)}$, both being about 0.3 V at 2.5 A. The Power MOS transistor (TMOS), with a typical On Resistance $r_{DS(on)}$ of about 1.1 Ω (1.5 Ω max) has an On voltage of about 2.8 V at 2.5 A, resulting in the higher case temperature. As the frequency is increased, the extremely fast switching MOSFET introduces little additional switching losses, resulting in a relatively constant case temperature.

The first generation SMI transistor shows the expected increasing temperature rise with increasing frequencies due to its relatively slow switching speed (the device was designed for 20 kHz applications). By contrast, the second generation Switchmode transistor MJ16004, which was designed for both higher fre-

FIGURE 2 — RESISTIVE LOAD SWITCHING OF DUTs AT 75 kHz

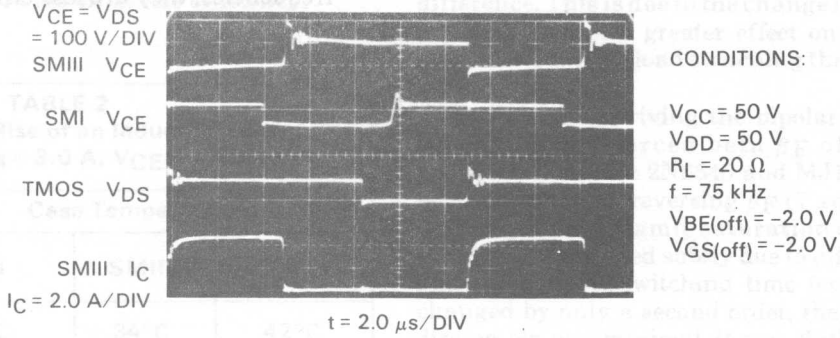
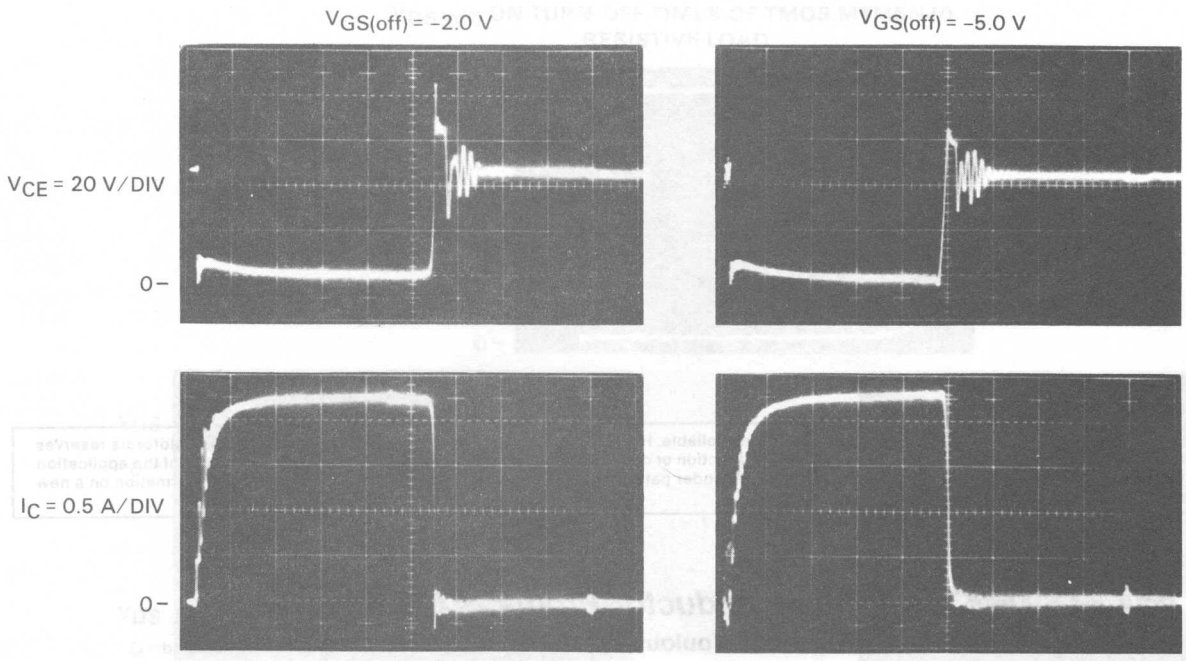


FIGURE 3 — RESISTIVE LOAD SWITCHING OF SMIII MJ16004 AT TWO OFF-BIAS VOLTAGES



quency operation and improved reverse bias safe operating area, shows a much lower case temperature rise; in fact, it typically operated cooler than the Power MOSFET up to the 75-100 kHz range.

The illustrated temperature rise curves were derived with typical devices. Testing of about ten sets of devices produced similar results, although in some cases, the effects of off-bias were not as pronounced due to slight differences in device processing and temperature measurement repeatability and accuracy, particularly where small differences in temperature had to be determined.

Although the curves show defined temperatures, the magnitude of the rise is only relative as it is obviously a function of the size and efficiency of the heat sink chosen. For this exercise, small heat sinks were chosen to raise the case temperature for higher differential temperature measurements. Secondly, the heat sinks (both the small ones for the DUTs and the large ones for the resistive and inductive loads) were thermally isolated from each other to minimize mutual thermal coupling effects; (the DUT heat sinks were mounted on ceramic standoffs and the load sinks on plastic washers to reduce thermal conduction to the chassis and hence to each device).

For clamped inductive loads, the greatest switching dissipation generally occurs during turn-off where the device, due to the rectangular load line, can be stressed simultaneously with both high current and voltage. The illustrated inductive loads simulate a flyback switching regulator where the energies stored in the inductors when the DUTs are turned on are transferred via their respective clamp diodes to the resistor-capacitor load during turn-off time. By proper selection of this load, the resulting clamp voltage was set for about 250 Vdc. The actual peak collector to emitter voltage V_{CEM} overshoot can be somewhat higher, being dependent on the rate of collector current fall-time t_{fi}, the forward recovery time of the clamp diode and the degree of proper RF layout (Figure 6). It is not uncommon for this overshoot to exceed the clamp supply voltage by 100 V or so.

An example of how reverse bias affects the switching speed, and thus efficiency, of the 2N6545 is shown in the photos of Figure 6. Note the difference in t_s, t_{fi}, V_{CEM} and collector emitter voltage rise time t_{rv}. At the optimum bias of about -5.0 V, the device turns off faster, there is less energy to be dissipated and a lower case temperature results. This is also true of the other two DUTs.

FIGURE 4 — TEMPERATURE RISE OF SWITCHMODE DEVICES AS A FUNCTION OF FREQUENCY

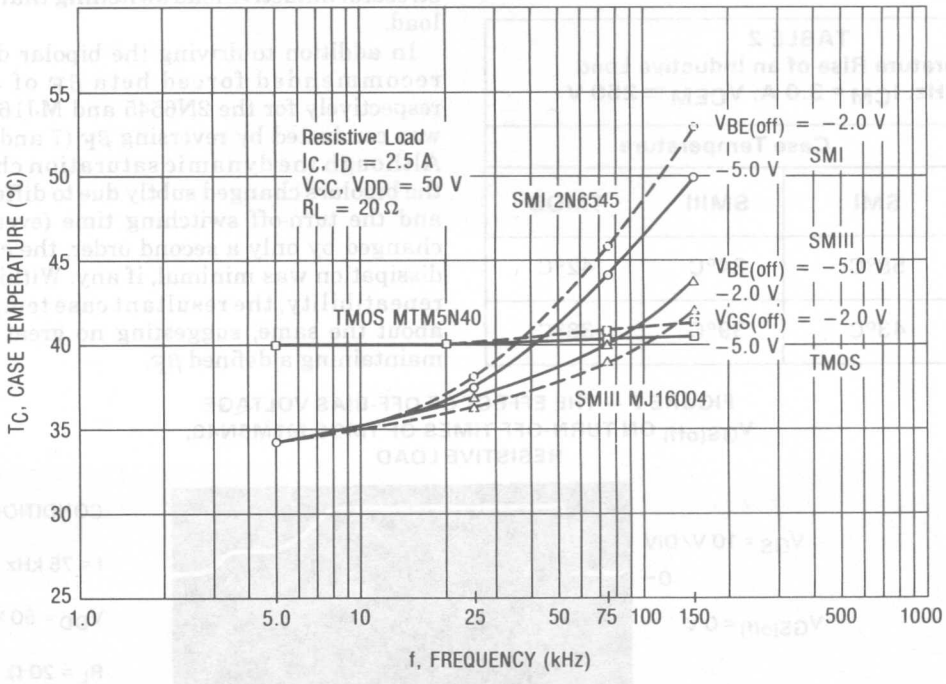


FIGURE 5 — CLAMPED INDUCTIVE LOAD SWITCHING WAVEFORMS OF TMOS MTM5N40

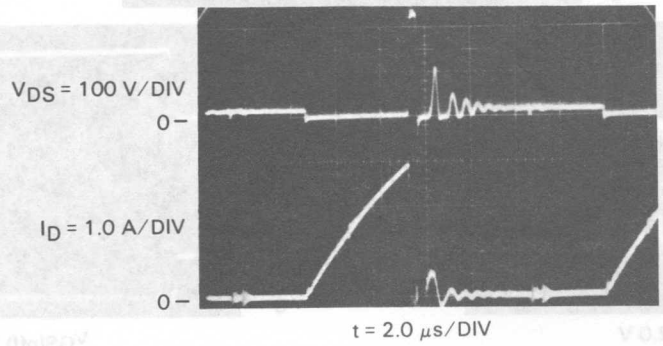
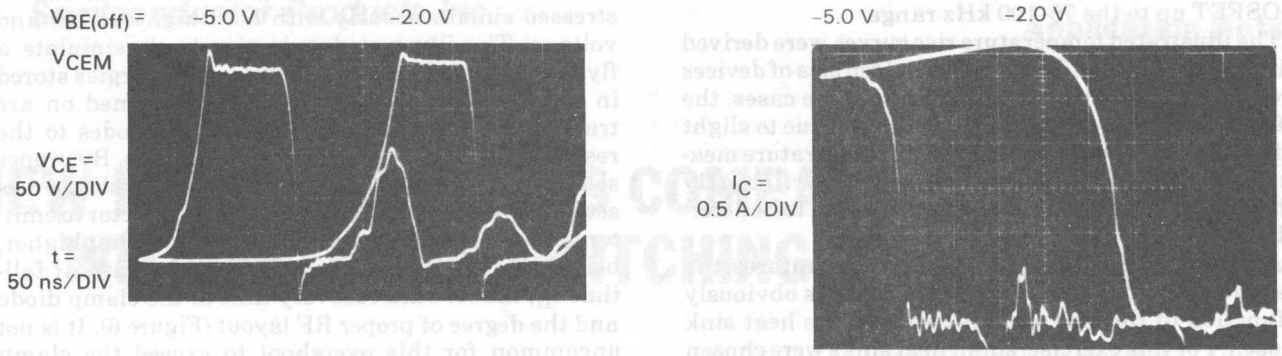


FIGURE 6 — CLAMPED INDUCTIVE LOAD TURN-OFF TIMES OF SMI 2N6545 WITH TWO OFF-BIAS VOLTAGES



Although there is no "storage time" associated with FETs, there is a turn-off delay time $t_{d(off)}$ due to device capacitances having to be discharged. The photos of Figure 7 describe the turn-off times when the off-bias is varied from 0 V, -2.0 V and -5.0 V respectively. As mentioned previously, the greater off-bias results in the lowest turn-off times.

The average temperature rise measurements of the three DUTs for the inductive load case (Table 2) illustrates the effect of off-bias on device efficiency.

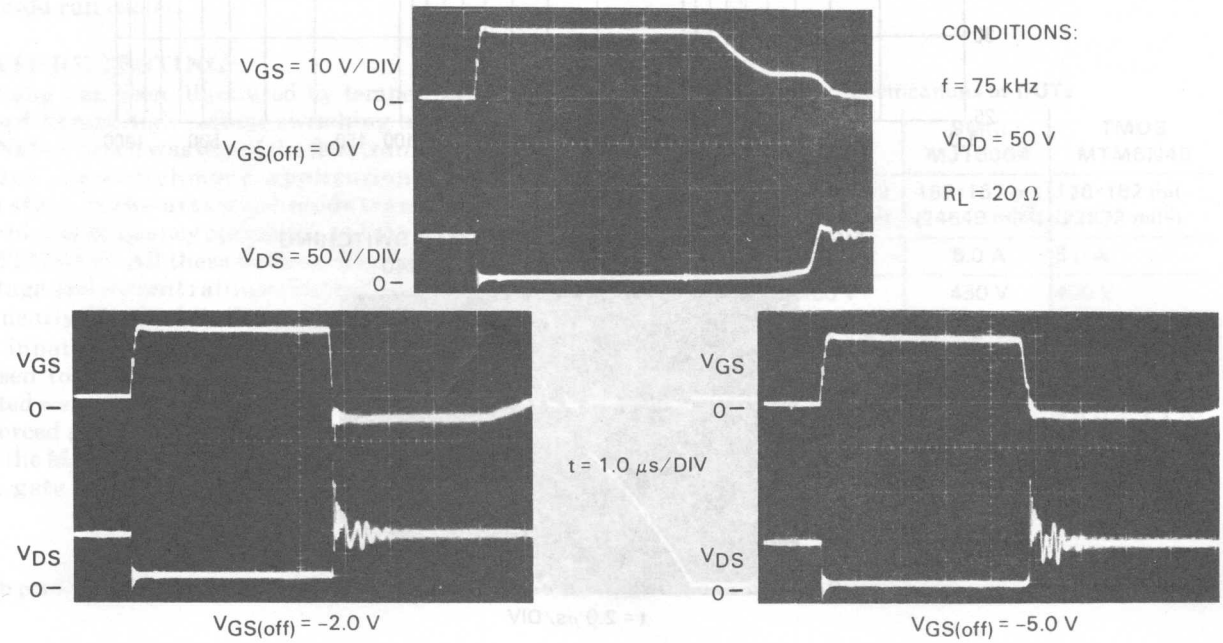
TABLE 2
Temperature Rise of an Inductive Load
f = 75 kHz, I_{CM} = 3.0 A, $V_{CEM} \cong$ 250 V

Off-Bias Voltage	Case Temperature		
	SMI	SMIII	TMOS
-2.0 V	58°C	34°C	42°C
-5.0 V	43°C	39°C	38°C

A direct point-by-point comparison between the inductive load and resistive load tests at 75 kHz can't be made since the respective load currents, and thus power dissipation are not the same. However, the trends can be compared; i.e., for the inductive load test, a greater temperature differential resulted between the optimum off-bias voltage and the second tested voltage, being as high as about 15°C for SMI. By comparison, the resistive load test showed only a few degrees difference. This is due to the change in turn-off switching time having a greater effect on the more energy stressful inductive load switching than on the resistive load.

In addition to driving the bipolar devices with the recommended forced beta β_F of about 5 and 7 respectively for the 2N6545 and MJ16004, a brief test was conducted by reversing β_F (7 and 5 respectively). Although the dynamic saturation characteristic of the bipolars changed subtly due to different base drive, and the turn-off switching time (even with off-bias) changed by only a second order, the change in power dissipation was minimal, if any. Within measurement repeatibility, the resultant case temperatures were about the same, suggesting no great requirement of maintaining a defined β_F.

FIGURE 7 — THE EFFECT OF OFF-BIAS VOLTAGE $V_{GS(off)}$ ON TURN-OFF TIMES OF TMOS MTM5N40, RESISTIVE LOAD



$V_{GS(off)}$ = -2.0 V

$V_{GS(off)}$ = -5.0 V

Examination of the above test results, the resistive temperature curves and the photos of the switching waveforms lead to the following conclusions about the switching efficiency of the test devices:

- Switchmode I 2N6545 can be comparably operated to 75 kHz when there is sufficient off-bias voltage (or reverse base current), approximately -5.0 V.
- For "real world" inductive loads, where the turn-off switching losses predominate, insufficient off-bias will produce excessive case temperature rise for SMI transistors (e.g., @ 75 kHz T_C = 58°C for $V_{BE(off)}$ = -2.0 V compared with 43°C for -5.0 V).
- Optimum off-bias will reduce turn-off switching speeds and thus switching losses for the bipolars and FET, but does not necessarily minimize the storage time (e.g., for SMIII, $t_{fi(min)}$ and $t_{s(min)}$ occur at about -2.0 V and -5.0 V respectively).
- At low frequencies, On (static) losses predominates; bipolars are thus more efficient than comparably sized Power MOSFETs.
- Power MOSFETS become more efficient at frequencies beyond about 100 kHz when compared to the new generation of switchmode bipolar transistors.
- Storage time, when it is not compensated for by circuit feedback techniques, somewhat affects efficiency at high frequencies due to increased On losses.
- Power MOSFETs have lower $t_{d(off)}$ when sufficiently reverse biased than bipolar t_s, thus allowing a higher operating frequency.
- Under optimum off-bias voltage conditions, the t_{fi} of SMIII approaches that of the very fast TMOS.
- Switchmode III MJ16004 compares favorably to Power MOSFET MTM5N40 at 75 kHz with an off-bias of -5.0 V and generally runs cooler at the optimum bias of -2.0 V (relative to -5.0 V for TMOS).
- Specified force beta β_F of the bipolars are not too critical for efficiency considerations as the turn-on times are partially dictated by the load. Off-bias tends to minimize the storage time effects as β_F is varied; however, excessive overdrive can cause I_C tail lifts during turn-off which may contribute to larger temperature rise.

The temperature rise results are a measure of total device dissipation, including the input drive loss. Even with the very large power gain of the high voltage MOSFETs (due to the high input impedance), at low frequencies, they are less efficient than the bipolars.

MOTOROLA *Semiconductor Products Inc.*
Avenue Général-Eisenhower - 31023 Toulouse CEDEX - FRANCE Printed in Switzerland